CLAIMS

What is claimed is:

1. A method comprising the steps of:

serially clocking a mask value through a plurality of serially coupled subscriber line interface circuits (SLICs) until each SLIC stores a corresponding portion of the mask value; and

serially communicating a command to the plurality of SLICs, wherein each SLIC responds to the command only if enabled by the corresponding portion of the mask value.

2. The method of claim 1 further comprising the step of:

providing the plurality of SLICs with data, wherein the mask value, the command, and the data are communicated on a same serial bus.

3. The method of claim 2 wherein the command is serially broadcast to the plurality of SLICs substantially simultaneously, wherein the data is serially broadcast to the plurality of SLICs substantially simultaneously.

4. The method of claim 2 wherein the mask value is a k-bit mask value, the command forms a portion of an m-bit command word, and the data is an n-bit data word, wherein the mask value, command word and data word have a same length (k=m=n).

5. The method of claim 1 wherein the command is a portion of a command word having a plurality of address bits identifying an address and a R/W bit to

indicate whether a read or write operation is to be performed on the identified address.

6. A method comprising the steps of:

initializing a plurality of subscriber line interface circuits (SLICs) to one of a first mode and a second mode;

serially clocking a mask value through the plurality of SLICs until each SLIC stores a corresponding portion of the mask value, if the plurality of SLICs is in the second mode; and

serially communicating a command to the plurality of SLICs, wherein every SLIC responds to the command when in the first mode, wherein only SLICs enabled by the corresponding portion of the mask value respond to the command when in the second mode.

7. The method of claim 6 further comprising the step of:

providing the plurality of SLICs with data, wherein the mask value, the command, and the data are communicated on a same serial bus.

8. The method of claim 7 wherein the command is serially broadcast to the plurality of SLICs substantially simultaneously, wherein the data is serially broadcast to the plurality of SLICs substantially simultaneously.

9. The method of claim 6 wherein the mask value is a *k*-bit mask value, the command forms a portion of an *m*-bit command word, and the data is an *n*-bit

data word, wherein the mask value, command word and data word have a same length (k=m=n).

10. The method of claim 6 wherein the command is a portion of a command word having a plurality of address bits identifying an address and a R/W bit to indicate whether a read or write operation is to be performed on the identified address.

11. An apparatus comprising:

a bus master;

a plurality of subscriber line interface circuits (SLICs); and

a bus coupling the serial devices to the bus master, wherein the bus master serially clocks a mask value through the plurality of serial devices until each serial device stores a portion of the mask value, wherein each of the plurality of serial devices responds to a subsequent command serially communicated by the bus master only if enabled by the corresponding portion of the mask value.

12. The apparatus of claim 11 wherein the bus master serially communicates data to the plurality of SLICs, wherein the mask value, the command, and the data are communicated on a same serial bus.

13. The apparatus of claim 12 wherein the bus master serially broadcasts the command to the plurality of SLICs substantially simultaneously, wherein the bus

master serially broadcasts the data to the plurality of SLICs substantially simultaneously.

14. The apparatus of claim 12 wherein the mask value is a *k*-bit mask value, the command forms a portion of an *m*-bit command word, and the data is an *n*-bit data word, wherein the mask value, command word and data word have a same length (*k*=*m*=*n*).

15. The apparatus of claim 11 wherein the command forms a portion of a command word having a plurality of address bits identifying an address and a R/W bit to indicate whether a read or write operation is to be performed on the identified address.

16. A subscriber line interface circuit (SLIC) apparatus comprising:

a memory coupled to receive a clock signal and a serial data in (SDI) signal carrying mask values, commands, and data, wherein the memory provides a clocked SDI signal;

a mode control providing a mode control signal; and

a multiplexer coupled to select one of the SDI signal and the clocked SDI signal as an SDI THRU signal in accordance with the mode control signal, wherein responsive to the mode control signal the multiplexer selects the clocked SDI signal as the SDI THRU signal when the SDI signal carries the mask value, wherein the multiplexer selects the SDI signal when the SDI signal carries commands or data.

17. The apparatus of claim 16 wherein the memory is a flip flop.

18. The apparatus of claim 16 wherein mask values are communicated as *k*-bit mask values, commands are communicated as a portion of *m*-bit command words, and data is communicated as *n*-bit data words, wherein the mask values, command words, and data words have a same length ($k=m=n$).

19. The apparatus of claim 16 wherein the commands are communicated as a portion of a command word having a plurality of address bits identifying an address and a R/W bit to indicate whether a read or write operation is to be performed on the identified address.

20. The apparatus of claim 16 wherein the mode control is configured to accommodate *k*-bit mask values, *m*-bit command words, and *n*-bit data words, wherein $k=m=n$.